WHAT IS CLAIMED:

1. A serial scaleable bandwidth interconnect bus for interconnection of physical layer and link layer devices, comprising:

(a) an ADD Bus operative to receive signals from said link layer devices and direct them to said physical layer devices; and

(b) a DROP Bus operative to receive signals from said physical layer devices and direct them to said link layer devices;

wherein said serial scaleable bandwidth interconnect bus is capable of supporting a plurality of links; and

wherein, for one or more of said links, ADD Bus timing control information is conveyed from said physical layer to said link layer in-band of said DROP Bus and independently of other ones of said links.

2. The interconnect bus according to claim 1, wherein said timing control information is 8B/10B encoded.

3. The interconnect bus according to claim 1, wherein said bus interface device supports fractional links.

4. The interconnect bus according to claim 1, wherein a bandwidth of each of said fractional links is an arbitary rate up to a maximum of approximately 45MB/s.

5. The interconnect bus according to claim 1, wherein said bus interface device supports T1s, E1s, TVT1.5s, TVT2s, DS3s, E3s or fractional links.

6. The interconnect bus according to claim 1, wherein said bus interface device supports 336 T1s, 252 E1s, 336 TVT1.5s, 252 TVT2s, 12 DS3s, 12E3s or 12 fractional links.

7. The interconnect bus according to claim 1, wherein said bus interface device is scaleable by increasing a serial interconnect rate in multiples of four.

8. The interconnect bus according to claim 1, wherein said bus interface device interconnects asynchronous and synchronous physical and link layer devices.

9. The interconnect bus according to claim 1, wherein said bus interface device is a LVDS interface.

10. The interconnect bus according to claim 1, wherein said DROP Bus comprises an in-band half-duplex channel for conveying control information between said physical layer and said link layer.

11. The interconnect bus according to claim 1, wherein said ADD Bus comprises an in-band half-duplex channel for conveying control information between said physical layer and said link layer.

12. An apparatus for providing a bus interface for interconnection of physical layer and link layer devices, comprising:

(a) an ADD Bus operative to receive signals from said link layer devices and direct them to said physical layer devices; and

(b) a DROP Bus operative to receive signals from said physical layer devices and direct them to said link layer devices;

wherein said apparatus is capable of supporting a plurality of links; and

wherein, for one or more of said links, ADD Bus timing control information is conveyed from said physical layer to said link layer in-band of said DROP Bus and independently of other ones of said links.

13. The apparatus according to claim 12, wherein said timing control information is 8B/10B encoded.

14. The apparatus according to claim 12, wherein said bus interface supports fractional links.

15. The apparatus according to claim 14, wherein a bandwidth of each of said fractional links is an arbitrary rate up to a maximum of approximately 45MB/s.

16. The apparatus according to claim 12, wherein said bus interface supports T1s, E1s, TVT1.5s, TVT2s, DS3s, E3s or fractional links.

17. The apparatus according to claim 12, wherein said bus interface supports 336 T1s, 252 E1s, 336 TVT1.5s, 252 TVT2s, 12 DS3s, 12E3s or 12 fractional links.

18. The apparatus according to claim 12, wherein said bus interface is scaleable by increasing a serial interconnect rate in multiples of four.

19. The apparatus according to claim 12, wherein said bus interface interconnects asynchronous and synchronous physical and link layer devices.

20. The apparatus according to claim 12, wherein said bus interface is a LVDS interface.

21. The apparatus according to claim 12, wherein said DROP Bus comprises an in-band half-duplex channel for conveying control information between said physical layer and said link layer.

22. The apparatus according to claim 12, wherein said ADD Bus comprises an in-band half-duplex channel for conveying control information between said physical layer and said link layer.

23. A method for connecting one or more Physical Layer devices with one or more link Layer devices, comprising:

(a) providing an ADD Bus operative to receive signals from said link layer devices and direct them to said physical layer devices; and

(b) providing a DROP Bus operative to receive signals from said physical layer devices and direct them to said link layer devices;

wherein said ADD Bus and said DROP Bus are capable of supporting a plurality of links; and

wherein, for one or more of said links, ADD Bus timing control information is conveyed from said physical layer to said link layer in-band of said DROP Bus and independently of other ones of said links.

24. The method of claim 23, wherein said timing control information is 8B/10B encoded.

25. The method of claim 23, wherein said ADD Bus and said DROP Bus support fractional links.

26. The method of claim 25, wherein a bandwidth of each of said fractional links is an arbitrary rate up to a maximum of approximately 45MB/s.

27. The method of claim 23, wherein said ADD Bus and said DROP Bus support T1s, E1s, TVT1.5s, TVT2s, DS3s, E3s or fractional links.

28. The method of claim 23, wherein said ADD Bus and said DROP Bus support 336 T1s, 252 E1s, 336 TVT1.5s, 252 TVT2s, 12 DS3s, 12E3s or 12 fractional links.

29. The method of claim 23, wherein said ADD Bus and said DROP Bus interconnect asynchronous and synchronous physical and link layer devices.

30. The method of claim 23, wherein said DROP Bus comprises an in-band half-duplex channel for conveying control information between said physical layer and said link layer.

31. The method of claim 23, wherein said ADD Bus comprises an in-band half-duplex channel for conveying control information between said physical layer and said link layer.